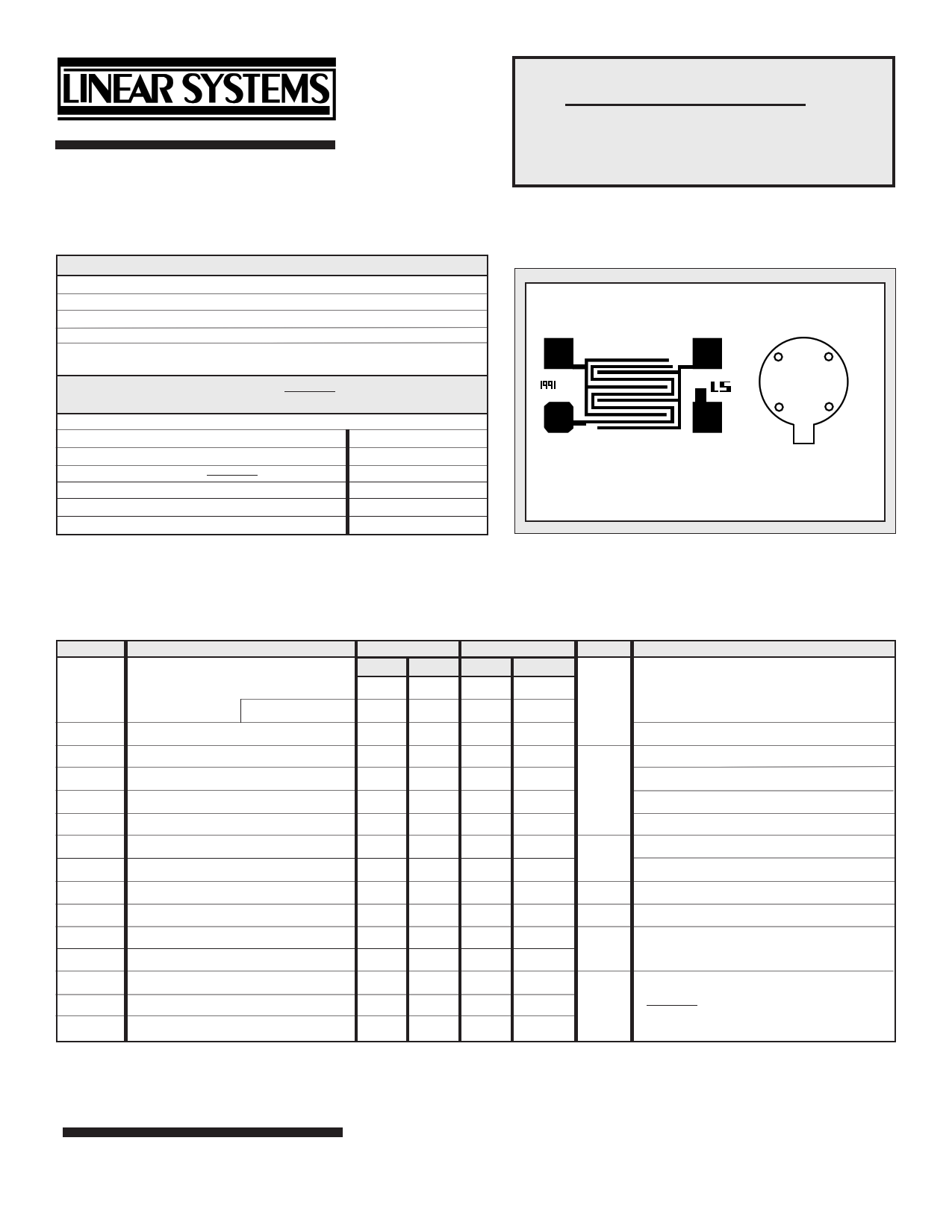
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.018”**

**.030”**



**D S**

**G Case**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**APPROVED BY: DK DIE SIZE .018” X .030” DATE: 4/18/18**

**MFG: LINEAR SYSTEMS THICKNESS .010” P/N: 3N163**

**DG 10.1.2**

#### Rev B, 7/19/02